IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 2, 3, 7, 8, and 9 and add new claim 10 in accordance with the following:

1. (CURRENTLY AMENDED) An automatic gain control circuit comprising:

a first error calculation circuit which calculates an amount of first error between an input signal and a first reference, and outputs a first signal corresponding to said first error;

a second error calculation circuit which calculates an amount of second error between an input signal and a second reference, and outputs a second signal corresponding to said second error;

a determination circuit connected to said first error calculation circuit and said second error calculation circuit, which determines a value of an output signal from said first error calculation circuit, and selects as an output signal of said determination circuit one of said first and second signals based on said determination; and

an integrator which integrates ~~an~~the output signal from said determination circuit.

2. (CURRENTLY AMENDED) ~~The~~ An automatic gain control circuit ~~according to Claim 1, further~~ comprising:

a first error calculation circuit which calculates an amount of first error between an input signal and a first reference, and outputs a first signal corresponding to said first error;

a second error calculation circuit which calculates an amount of second error between an input signal and a second reference, and outputs a second signal corresponding to said second error;

a determination circuit connected to said first error calculation circuit and said second error calculation circuit, determines a value of an output signal from said first error calculation circuit, and selects as an output signal of said determination circuit one of said first and second signals based on said determination;

an integrator integrates the output signal from said determination circuit; and

a first multiplier and a second multiplier connected to an output port of said first error calculation circuit and said second error calculation circuit respectively;

wherein said determination circuit outputs, based on said determination of said output signal from said first error calculation circuit, a signal of an amount of 1 to one of said first or second multiplier, and a signal of an amount of 0 to said other one of said first or second multiplier.

3. (CURRENTLY AMENDED) ~~The~~ An automatic gain control circuit ~~according to Claim 1, further~~ comprising:

a first error calculation circuit which calculates an amount of first error between an input signal and a first reference, and outputs a first signal corresponding to said first error;

a second error calculation circuit which calculates an amount of second error between an input signal and a second reference, and outputs a second signal corresponding to said second error;

a determination circuit connected to said first error calculation circuit and said second error calculation circuit, determines a value of an output signal from said first error calculation circuit, and selects as an output signal of said determination circuit one of said first and second signals based on said determination;

an integrator integrates the output signal from said determination circuit; and

a first AND circuit and a second AND circuit connected to an output port of said first error calculation circuit and said second error calculation circuit respectively;

wherein said determination circuit outputs, based on said determination of said output signal from said first error calculation circuit, a signal of an amount of 1 to one of said first or second AND circuit, and a signal of an amount of 0 to said other one of said first or second AND circuit.

4. (ORIGINAL) A data communications device comprising:

an equalizer for equalizing an input signal from a communication line;

an automatic gain controller, connected to said equalizer, to control a level of an input signal to be stabilized in a constant value;

wherein, said automatic gain controller comprising:

a first error calculation circuit for calculating a first error value between an input signal and a first reference signal;

a second error calculation circuit for calculating a second error value between an input

signal and a second reference signal;

an integrating circuit connected to said first or second error calculation circuits, for integrating a difference between a level of an input signal and a predetermined value; and

a determination module, connected to said first error calculation circuit, said second error calculation circuit and said integrating circuit, for determining whether an output signal of said integrating circuit is larger than said predetermined value, and selecting one of said first error calculation circuit and said second error calculation circuit for an automatic gain control based on said determination.

5. (ORIGINAL) The data communications device according to Claim 4, wherein:

said first error calculation circuit comprising a squaring circuit for squaring an input signal; and

a comparator for comparing a difference between said squared signal and a reference signal.

6. (ORIGINAL) The data communications device according to Claim 4 or Claim 5, wherein:

said second error calculation circuit comprising a rectifying circuit for rectifying an input signal; and

a comparator for comparing a difference between said rectified signal and a reference signal.

7. (CURRENTLY AMENDED) An automatic gain control circuit comprising:

a first error calculation circuit ~~for~~ calculating a first error amount between a power of an input signal and an average power of an eye pattern;

a second error calculation circuit ~~for~~ calculating a second error amount between a product of an input signal and a rectifying signal and a product of an ideal signal and a rectifying signal;

a first integrator ~~for~~ integrating said first error amount;

a determination module connected to said first error calculation circuit, said second calculation circuit and said first integrator, ~~for~~ determining whether said integrated error amount exceeds an average power of an eye pattern, and ~~output~~ outputting said first error amount when it is determined that said integrated first error amount exceeds said average power of an eye pattern, and ~~output~~ outputting said second error amount when it is determined that said

integrated error amount does not exceed said average power of an eye pattern; and

a second integrator ~~for~~ integrating an output signal from said determination module.

8. (CURRENTLY AMENDED) An automatic gain control method comprising:

calculating a first error between an input signal and a first reference;

calculating a second error between an input signal and a second reference;

determining a value of said first error;

selecting one of said first error and said second error as an output based on said determination; and

integrating the selected output .

9. (CURRENTLY AMENDED) An automatic gain control method, comprising:

calculating a first error between a power of an input signal and an average power of an eye pattern;

calculating a second error between a product of an input signal and a rectifying signal and a product of an ideal signal and a rectifying signal;

integrating said first error;

determining whether said integrated first error exceeds said average power of an eye pattern;

~~output~~ outputting said first error when said integrated first error exceeds said average power, and ~~output~~ outputting said second error when said integrated first error does not exceeds said average power; and

integrating said output first or second error.

10. (NEW) An automatic gain control circuit comprising:

error calculation circuits calculating respective amounts of error between portions of an input signal and corresponding error references, and outputting error signals corresponding to the respective amounts of error; and

a determination circuit connected to the error calculation circuits and determining a value of an output error signal from one of the error calculation circuits, and selecting as an output signal from said determination circuit one of the output error signals based on said determination; and

an integrator coupled to the determination circuit and integrating the output error signal output from said determination circuit.